

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

As demonstrated in the chart below, ASUS directly and indirectly infringes at least claim 7 of US 7,532,808 (the “’808 Patent”). ASUS directly infringes, contributes to the infringement of, and/or induces infringement of the ’808 Patent by making, using, selling, offering for sale, and/or importing into the United States the Accused Products that are covered by at least claim 7 of the ’808 Patent. The Accused Products are devices that decode H.264-compliant video. For example, ASUS Q543MV Notebook (“ASUS Q543MV”) is a representative product for other ASUS devices that decode H.264-compliant video.

The ASUS Q543MV contains at least one video decoder that helps decode H.264-compliant video.¹ While evidence from the ASUS Q543MV is specifically charted herein, the evidence and contentions charted herein apply equally to the other ASUS Accused Products that decode H.264-compliant video.

No part of this exemplary chart construes, or is intended to construe, the specification, file history, or claims of the ’808 Patent. Moreover, this exemplary chart does not limit, and is not intended to limit, Nokia’s infringement positions or contentions.

The following infringement chart includes exemplary citations to ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audiovisual services (available at <https://www.itu.int/rec/T-REC-H.264-200503-S/en>) (the “H.264 Standard”). The cited functionality has been included in editions of the H.264 Standard since at least May 2003 and remains in current editions of the H.264 Standard. Any ASUS device that includes a decoder that practices the functionality in any of these editions of the H.264 Standard (“H.264 Decoder”) practices at least claim 7 of the ’808 Patent.

Nokia contends each of the following limitations is met literally, and, to the extent a limitation is not met literally, it is met under the doctrine of equivalents.²

¹ See, e.g., <https://www.asus.com/us/laptops/for-home/everyday-use/asus-vivobook-pro-15-oled-q543/techspec/>; <https://www.intel.com/content/www/us/en/products/sku/236849/intel-core-ultra-9-processor-185h-24m-cache-up-to-5-10-ghz/specifications.html>; <https://developer.nvidia.com/video-encode-and-decode-gpu-support-matrix-new>.

² This claim chart is based on the information currently available to Nokia and is intended to be exemplary in nature. Nokia reserves all rights to update and elaborate its infringement positions, including as Nokia obtains additional information during the course of discovery.

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

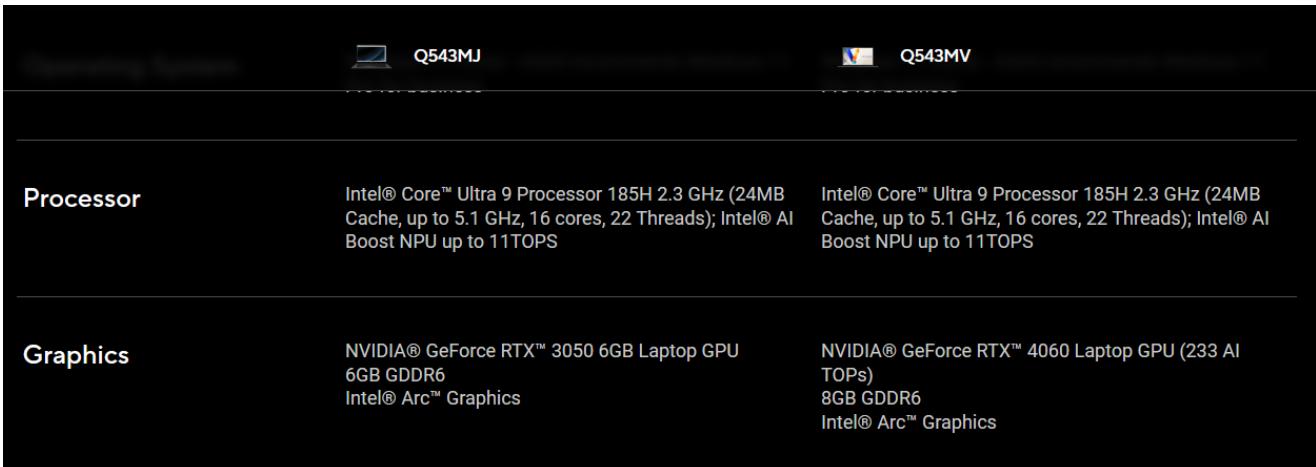
U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS										
7. [A] A method of decoding an encoded video sequence, the method comprising:	<p>Each of the Accused Products, such as the ASUS Q543MV, performs a method of decoding an encoded video sequence.</p> <p>For example, and without limitation, the Asus Q543MV uses hardware-accelerated decoding and includes an NVIDIA GeForce RTX 4060 Laptop graphics processing unit (“GPU”) and an Intel Core Ultra 9 Processor 185H.</p>  <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; background-color: black; color: white;">Processor</th> <th style="text-align: center;">Q543MJ</th> <th style="text-align: center;">Q543MV</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Processor</td> <td style="text-align: center;">Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS</td> <td style="text-align: center;">Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS</td> </tr> <tr> <td style="text-align: center;">Graphics</td> <td style="text-align: center;">NVIDIA® GeForce RTX™ 3050 6GB Laptop GPU 6GB GDDR6 Intel® Arc™ Graphics</td> <td style="text-align: center;">NVIDIA® GeForce RTX™ 4060 Laptop GPU (233 AI TOPs) 8GB GDDR6 Intel® Arc™ Graphics</td> </tr> </tbody> </table> <p>Source: https://www.asus.com/us/laptops/for-home/everyday-use/asus-vivobook-pro-15-oled-q543/techspec/ (last accessed March 6, 2025).</p>		Processor	Q543MJ	Q543MV	Processor	Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS	Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS	Graphics	NVIDIA® GeForce RTX™ 3050 6GB Laptop GPU 6GB GDDR6 Intel® Arc™ Graphics	NVIDIA® GeForce RTX™ 4060 Laptop GPU (233 AI TOPs) 8GB GDDR6 Intel® Arc™ Graphics
Processor	Q543MJ	Q543MV									
Processor	Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS	Intel® Core™ Ultra 9 Processor 185H 2.3 GHz (24MB Cache, up to 5.1 GHz, 16 cores, 22 Threads); Intel® AI Boost NPU up to 11TOPS									
Graphics	NVIDIA® GeForce RTX™ 3050 6GB Laptop GPU 6GB GDDR6 Intel® Arc™ Graphics	NVIDIA® GeForce RTX™ 4060 Laptop GPU (233 AI TOPs) 8GB GDDR6 Intel® Arc™ Graphics									
	H.264 Hardware Encode/Decode ?	Yes									
	H.265 (HEVC) Hardware Encode/Decode ?	Yes									
	AV1 Encode/Decode ?	Yes									

EXHIBIT 16
UNITED STATES PATENT NO. 7,532,808
CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS

EXHIBIT 16
UNITED STATES PATENT No. 7,532,808
CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS

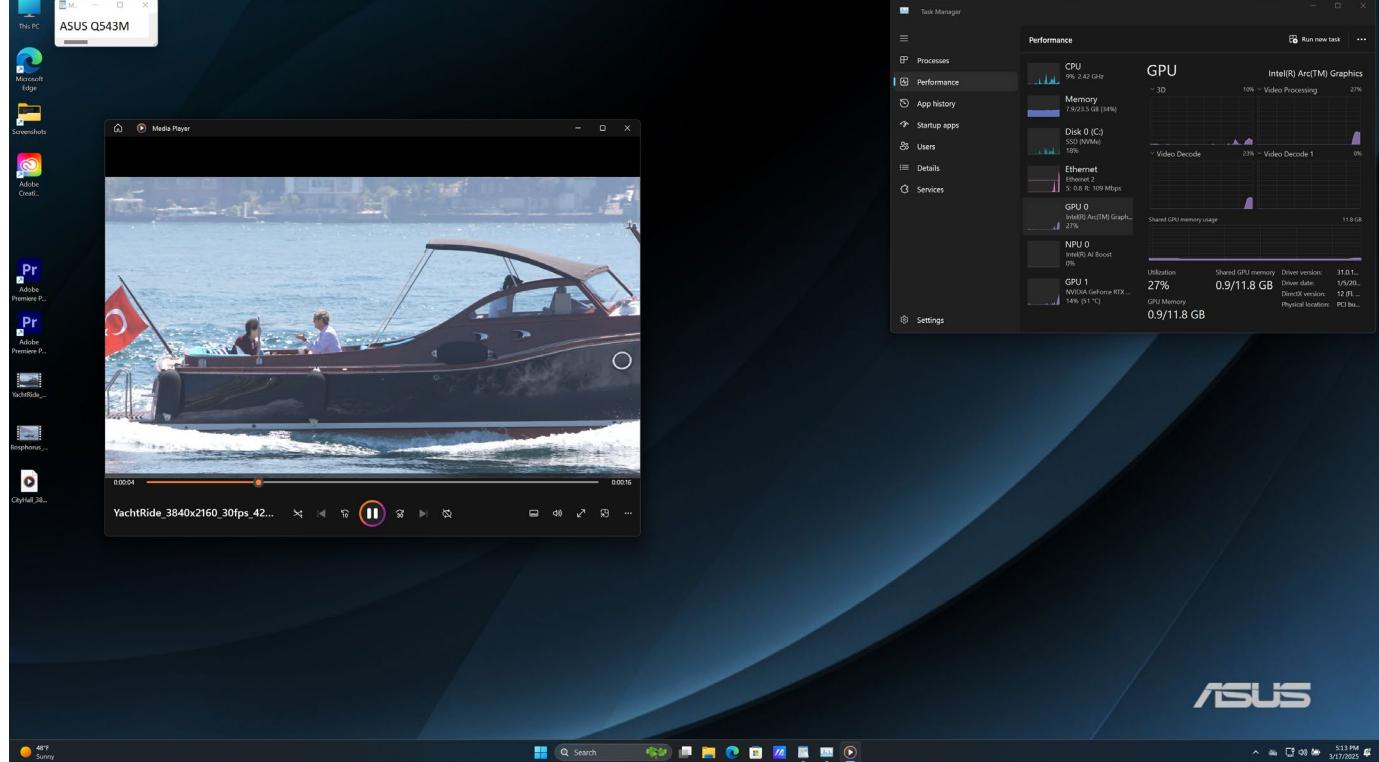
U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	 <p>The screenshot displays a Windows desktop environment. On the left is a Start menu with various application icons. In the center, a Media Player window is open, showing a video of two people on a boat. The video player interface includes a play/pause button, a progress bar from 0:00:04 to 0:00:10, and other standard media controls. To the right of the video player is the Windows Task Manager, which provides real-time system performance data. The Task Manager shows CPU usage at 9%, GPU usage for Intel(R) Arc(TM) Graphics at 27%, and GPU 0 usage for NVIDIA GeForce RTX 3070 at 27%. Other tabs in the Task Manager include Processes, Performance, App history, Startup apps, Users, Details, Services, and Settings. The desktop background features a dark blue gradient with the 'ASUS' logo in the bottom right corner. At the bottom of the screen is the Windows taskbar with various pinned icons.</p> <p>Source: Screenshot of H.264-compliant video playback on ASUS Q543MV.</p> <p>The following specifications provide further evidence of how the Accused Products operate:</p> <p>0.2 Purpose ... This Recommendation International Standard was developed in response to the growing need for higher compression of moving pictures for various applications such as videoconferencing, digital storage media, television broadcasting, internet streaming, and communication. It is also designed</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>to enable the use of the coded video representation in a flexible manner for a wide variety of network environments. The use of this Recommendation International Standard allows motion video to be manipulated as a form of computer data and to be stored on various storage media, transmitted and received over existing and future networks and distributed on existing and future broadcasting channels.</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at p. 1).</p> <p>3 Definitions</p> <p>For the purposes of this Recommendation International Standard, the following definitions apply.</p> <p>...</p> <p>3.1 access unit: A set of <i>NAL units</i> always containing exactly one <i>primary coded picture</i>. In addition to the <i>primary coded picture</i>, an access unit may also contain one or more <i>redundant coded pictures</i> or other <i>NAL units</i> not containing <i>slices</i> or <i>slice data partitions</i> of a <i>coded picture</i>. The decoding of an access unit always results in a <i>decoded picture</i>.</p> <p>...</p> <p>3.14 bitstream: A sequence of bits that forms the representation of <i>coded pictures</i> and associated data forming one or more <i>coded video sequences</i>. Bitstream is a collective term used to refer either to a <i>NAL unit stream</i> or a <i>byte stream</i>.</p> <p>...</p> <p>3.27 coded picture: A <i>coded representation</i> of a <i>picture</i> ...</p> <p>...</p> <p>3.30 coded video sequence: A sequence of <i>access units</i> that consists, in decoding order, of an <i>IDR access unit</i> followed by zero or more non-IDR <i>access units</i> including all subsequent <i>access units</i> up to but not including any subsequent <i>IDR access unit</i>.</p> <p>...</p> <p>3.37 decoded picture: A <i>decoded picture</i> is derived by decoding a <i>coded picture</i>. A <i>decoded picture</i> is either a <i>decoded frame</i>, or a <i>decoded field</i>. A <i>decoded field</i> is either a <i>decoded top field</i> or a <i>decoded bottom field</i>.</p> <p>...</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>3.41 decoding process: The process specified in this Recommendation International Standard that reads a <i>bitstream</i> and derives <i>decoded pictures</i> from it.</p> <p>...</p> <p>3.109 primary coded picture: The coded representation of a <i>picture</i> to be used by the <i>decoding process</i> for a bitstream conforming to this Recommendation International Standard. The primary coded picture contains all <i>macroblocks</i> of the <i>picture</i>. The only <i>pictures</i> that have a normative effect on the <i>decoding process</i> are primary coded pictures. See also <i>redundant coded picture</i>.</p> <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 4–6).</p>
<p>[B] receiving an indication of a skip coding mode for a first segment;</p>	<p>Each of the Accused Products, such as the ASUS Q543MV, performs a method of decoding an encoded video sequence, the method comprising receiving an indication of a skip coding mode for a first segment.</p> <p>For example, and without limitation, the H.264 Standard specifies the following regarding the decoding process. For example, as defined in Subclause 7.3.4, the Slice Layer Syntax includes a syntax element <code>mb_skip_run</code> (when CAVLC entropy coding is used) or <code>mb_skip_flag</code> (in the case of CABAC entropy coding). For P and SP slices, for example, a value of <code>mb_skip_flag</code> equal to 1 indicates that a macroblock has been coded as a skipped macroblock or, correspondingly, a value of <code>mb_skip_run</code> greater than zero indicates that a number of consecutive macroblocks has been coded as skipped macroblocks (see definition in Subclause 3.135). Upon receiving such an indication, an H.264-compliant decoder infers that <code>mb_type</code> for the current macroblock is <code>P_Skip</code> (Table 7-13). The following specifications provide further evidence of how the Accused Products operate:</p> <p>3 Definitions</p> <p>For the purposes of this Recommendation International Standard, the following definitions apply.</p> <p>...</p> <p>3.15 block: An MxN (M-column by N-row) array of samples, or an MxN array of <i>transform coefficients</i>.</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>...</p> <p>3.24 chroma: An adjective specifying that a sample array or single sample is representing one of the two colour difference signals related to the primary colours. The symbols used for a chroma array or sample are Cb and Cr.</p> <p>...</p> <p>3.74 luma: An adjective specifying that a sample array or single sample is representing the monochrome signal related to the primary colours. The symbol or subscript used for luma is Y or L.</p> <p>...</p> <p>3.75 macroblock: A 16x16 <i>block</i> of <i>luma</i> samples and two corresponding <i>blocks</i> of <i>chroma</i> samples</p> <p>...</p> <p>3.135 skipped macroblock: A <i>macroblock</i> for which no data is coded other than an indication that the <i>macroblock</i> is to be decoded as "skipped". This indication may be common to several <i>macroblocks</i>.</p> <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 8–11).</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS****7.3.4 Slice data syntax**

	C	Descriptor
slice_data() {		
if(entropy_coding_mode_flag)		
while(!byte_aligned())		
cabac_alignment_one_bit	2	f(1)
CurrMbAddr = first_mb_in_slice * (1 + MbaffFrameFlag)		
moreDataFlag = 1		
prevMbSkipped = 0		
do {		
if(slice_type != I && slice_type != SI)		
if(!entropy_coding_mode_flag) {		
mb_skip_run	2	ue(v)
prevMbSkipped = (mb_skip_run > 0)		
for(i=0; i<mb_skip_run; i++)		
CurrMbAddr = NextMbAddress(CurrMbAddr)		
moreDataFlag = more_rbsp_data()		
} else {		
mb_skip_flag	2	ae(v)
moreDataFlag = !mb_skip_flag		
}		

(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at p. 49).

7.4.4 Slice data semantics

...

mb_skip_run specifies the number of consecutive skipped macroblocks for which, when decoding a P or SP slice, **mb_type** shall be inferred to be **P_Skip** and the macroblock type is collectively referred to as a P macroblock type . . .

...

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>mb_skip_flag equal to 1 specifies that for the current macroblock, when decoding a P or SP slice, mb_type shall be inferred to be P_Skip and the macroblock type is collectively referred to as P macroblock type . . .</p> <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at p. 85).</p> <p>7.4.5 Macroblock layer semantics</p> <p>mb_type specifies the macroblock type. The semantics of mb_type depend on the slice type.</p> <p>...</p> <p>Macroblock types that may be collectively referred to as P macroblock types are specified in Table 7-13.</p> <p>...</p> <p style="text-align: center;">Table 7-13 – Macroblock type values 0 to 4 for P and SP slices</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS																																																	
	<table border="1" data-bbox="897 287 1685 840"> <thead> <tr> <th data-bbox="897 287 973 551">mb_type</th><th data-bbox="973 287 1100 551">Name of mb_type</th><th data-bbox="1100 287 1220 551">NumMbPart (mb_type)</th><th data-bbox="1220 287 1341 551">MbPartPredMode (mb_type, 0)</th><th data-bbox="1341 287 1461 551">MbPartPredMode (mb_type, 1)</th><th data-bbox="1461 287 1603 551">MbPartWidth (mb_type)</th><th data-bbox="1603 287 1723 551">MbPartHeight (mb_type)</th></tr> </thead> <tbody> <tr> <td data-bbox="897 551 973 589">0</td><td data-bbox="973 551 1100 589">P_L0_16x16</td><td data-bbox="1100 551 1220 589">1</td><td data-bbox="1220 551 1341 589">Pred_L0</td><td data-bbox="1341 551 1461 589">na</td><td data-bbox="1461 551 1603 589">16</td><td data-bbox="1603 551 1723 589">16</td></tr> <tr> <td data-bbox="897 589 973 626">1</td><td data-bbox="973 589 1100 626">P_L0_L0_16x8</td><td data-bbox="1100 589 1220 626">2</td><td data-bbox="1220 589 1341 626">Pred_L0</td><td data-bbox="1341 589 1461 626">Pred_L0</td><td data-bbox="1461 589 1603 626">16</td><td data-bbox="1603 589 1723 626">8</td></tr> <tr> <td data-bbox="897 626 973 664">2</td><td data-bbox="973 626 1100 664">P_L0_L0_8x16</td><td data-bbox="1100 626 1220 664">2</td><td data-bbox="1220 626 1341 664">Pred_L0</td><td data-bbox="1341 626 1461 664">Pred_L0</td><td data-bbox="1461 626 1603 664">8</td><td data-bbox="1603 626 1723 664">16</td></tr> <tr> <td data-bbox="897 664 973 701">3</td><td data-bbox="973 664 1100 701">P_8x8</td><td data-bbox="1100 664 1220 701">4</td><td data-bbox="1220 664 1341 701">na</td><td data-bbox="1341 664 1461 701">na</td><td data-bbox="1461 664 1603 701">8</td><td data-bbox="1603 664 1723 701">8</td></tr> <tr> <td data-bbox="897 701 973 739">4</td><td data-bbox="973 701 1100 739">P_8x8ref0</td><td data-bbox="1100 701 1220 739">4</td><td data-bbox="1220 701 1341 739">na</td><td data-bbox="1341 701 1461 739">na</td><td data-bbox="1461 701 1603 739">8</td><td data-bbox="1603 701 1723 739">8</td></tr> <tr> <td data-bbox="897 739 973 776">inferred</td><td data-bbox="973 739 1100 776">P_Skip</td><td data-bbox="1100 739 1220 776">1</td><td data-bbox="1220 739 1341 776">Pred_L0</td><td data-bbox="1341 739 1461 776">na</td><td data-bbox="1461 739 1603 776">16</td><td data-bbox="1603 739 1723 776">16</td></tr> </tbody> </table>	mb_type	Name of mb_type	NumMbPart (mb_type)	MbPartPredMode (mb_type, 0)	MbPartPredMode (mb_type, 1)	MbPartWidth (mb_type)	MbPartHeight (mb_type)	0	P_L0_16x16	1	Pred_L0	na	16	16	1	P_L0_L0_16x8	2	Pred_L0	Pred_L0	16	8	2	P_L0_L0_8x16	2	Pred_L0	Pred_L0	8	16	3	P_8x8	4	na	na	8	8	4	P_8x8ref0	4	na	na	8	8	inferred	P_Skip	1	Pred_L0	na	16	16
mb_type	Name of mb_type	NumMbPart (mb_type)	MbPartPredMode (mb_type, 0)	MbPartPredMode (mb_type, 1)	MbPartWidth (mb_type)	MbPartHeight (mb_type)																																												
0	P_L0_16x16	1	Pred_L0	na	16	16																																												
1	P_L0_L0_16x8	2	Pred_L0	Pred_L0	16	8																																												
2	P_L0_L0_8x16	2	Pred_L0	Pred_L0	8	16																																												
3	P_8x8	4	na	na	8	8																																												
4	P_8x8ref0	4	na	na	8	8																																												
inferred	P_Skip	1	Pred_L0	na	16	16																																												
	<p>The following semantics are assigned to the macroblock types in Table 7-13.</p> <p>...</p> <ul style="list-style-type: none"> – P_Skip: no further data is present for the macroblock in the bitstream. <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 85, 88–89).</p>																																																	
[C] assigning either a zero motion vector or a predicted non-zero motion vector for the skip coding mode for the first segment based at least in part on the motion	<p>Each of the Accused Products, such as the ASUS Q543MV, performs a method of decoding an encoded video sequence, the method comprising assigning either a zero motion vector or a predicted non-zero motion vector for the skip coding mode for the first segment based at least in part on the motion information of a second segment neighboring the first segment.</p>																																																	

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

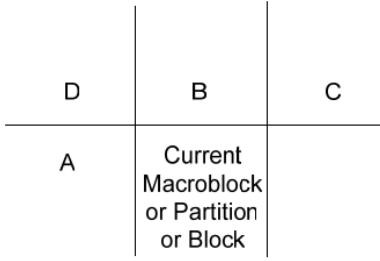
U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
<p>information of a second segment neighboring the first segment; and</p>	<p>For example, and without limitation, the H.264 Standard specifies the following regarding the decoding process and H.264-compliant bitstream. For example, the H.264/AVC Standard describes the derivation process for luma motion vectors for skipped macroblocks in P and SP slices in Subclause 8.4.1.1. Subclause 8.4.1.1 specifies that depending on the values of motion vectors in the neighbouring blocks to the left of the current macroblock and above the current macroblock, the current macroblock will be assigned either a zero-value or a non-zero value motion vector. By way of example, for a non-zero luma motion vector, the decoder predicts its value based on motion data of neighbouring blocks. The following specifications provide further evidence of how the Accused Products operate:</p> <p style="text-align: center;">6.4.8 Derivation processes for neighbouring macroblocks, blocks, and partitions</p> <p style="text-align: center;">...</p> <p>Figure 6-14 illustrates the relative location of the neighbouring macroblocks, blocks, or partitions A, B, C, and D to the current macroblock, partition, or block, when the current macroblock, partition, or block is in frame coding mode.</p>  <p>Figure 6-14 – Determination of the neighbouring macroblock, blocks, and partitions (informative)</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 28–29)</p> <p>8.4.1 Derivation process for motion vector components and reference indices</p> <p>Inputs to this process are</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<ul style="list-style-type: none"> – a macroblock partition mbPartIdx, – a sub-macroblock partition subMbPartIdx. <p>Outputs of this process are</p> <ul style="list-style-type: none"> – luma motion vectors mvL0 and mvL1 as well as the chroma motion vectors mvCL0 and mvCL1 – reference indices refIdxL0 and refIdxL1 – prediction list utilization flags predFlagL0 and predFlagL1 – a sub-partition macroblock motion vector count variable subMvCnt <p>For the derivation of the variables mvL0 and mvL1 as well as refIdxL0 and refIdxL1, the following applies.</p> <ul style="list-style-type: none"> – If mb_type is equal to P_Skip, the derivation process for luma motion vectors for skipped macroblocks in P and SP slices in subclause 8.4.1.1 is invoked with the output being the luma motion vectors mvL0 and reference indices refIdxL0, and predFlagL0 is set equal to 1. mvL1 and refIdxL1 are marked as not available and predFlagL1 is set equal to 0. The sub-partition motion vector count variable subMvCnt is set equal to 1. – Otherwise, if mb_type is equal to B_Skip or B_Direct_16x16 or sub_mb_type[mbPartIdx] is equal to B_Direct_8x8, the derivation process for luma motion vectors for B_Skip, B_Direct_16x16, and B_Direct_8x8 in B slices in subclause 8.4.1.2 is invoked with mbPartIdx and subMbPartIdx as the input and the output being the luma motion vectors mvL0, mvL1, the reference indices refIdxL0, refIdxL1, the sub-partition motion vector count subMvCnt, and the prediction utilization flags predFlagL0 and predFlagL1. – Otherwise, for X being replaced by either 0 or 1 in the variables predFlagLX, mvLX, refIdxLX, and in Pred_LX and in the syntax elements ref_idx_IX and mvd_IX, the following applies. <p style="text-align: center;">...</p> <p>8.4.1.1 Derivation process for luma motion vectors for skipped macroblocks in P and SP slices</p> <p>This process is invoked when mb_type is equal to P_Skip.</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>Outputs of this process are the motion vector mvL0 and the reference index refIdxL0.</p> <p>The reference index refIdxL0 for a skipped macroblock is derived as follows.</p> $\text{refIdxL0} = 0.$ <p>For the derivation of the motion vector mvL0 of a P_Skip macroblock type, the following applies.</p> <ul style="list-style-type: none"> – The process specified in subclause 8.4.1.3.2 is invoked with mbPartIdx set equal to 0, subMbPartIdx set equal to 0, currSubMbType set equal to "na", and listSuffixFlag set equal to 0 as input and the output is assigned to mbAddrA, mbAddrB, mvL0A, mvL0B, refIdxL0A, and refIdxL0B. – The variable mvL0 is specified as follows. <ul style="list-style-type: none"> – If any of the following conditions are true, both components of the motion vector mvL0 are set equal to 0. <ul style="list-style-type: none"> – mbAddrA is not available – mbAddrB is not available – refIdxL0A is equal to 0 and both components of mvL0A are equal to 0 – refIdxL0B is equal to 0 and both components of mvL0B are equal to 0 – Otherwise, the derivation process for luma motion vector prediction as specified in subclause 8.4.1.3 is invoked with mbPartIdx = 0, subMbPartIdx = 0, refIdxL0, and currSubMbType = "na" as inputs and the output is assigned to mvL0. <p>NOTE – The output is directly assigned to mvL0, since the predictor is equal to the actual motion vector.</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 137–39).</p> <p>8.4.1.3 Derivation process for luma motion vector prediction</p> <p>Inputs to this process are</p> <ul style="list-style-type: none"> – the macroblock partition index mbPartIdx, – the sub-macroblock partition index subMbPartIdx,

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<ul style="list-style-type: none"> – the reference index of the current partition refIdxLX (with X being 0 or 1), – the variable currSubMbType. <p>Output of this process is the prediction mvpLX of the motion vector mvLX (with X being 0 or 1). The derivation process for the neighbouring blocks for motion data in subclause 8.4.1.3.2 is invoked with mbPartIdx, subMbPartIdx, currSubMbType, and listSuffixFlag = X (with X being 0 or 1 for refIdxLX being refIdxL0 or refIdxL1, respectively) as the input and with mbAddrN\mbPartIdxN\subMbPartIdxN, reference indices refIdxLXN and the motion vectors mvLXN with N being replaced by A, B, or C as the output.</p> <p>The derivation process for median luma motion vector prediction in subclause 8.4.1.3.1 is invoked with mbAddrN\mbPartIdxN\subMbPartIdxN, mvLXN, refIdxLXN with N being replaced by A, B, or C and refIdxLX as the input and mvpLX as the output, unless one of the following is true.</p> <ul style="list-style-type: none"> – MbPartWidth(mb_type) is equal to 16, MbPartHeight(mb_type) is equal to 8, mbPartIdx is equal to 0, and refIdxLXB is equal to refIdxLX, $\text{mvpLX} = \text{mvLXB}$ – MbPartWidth(mb_type) is equal to 16, MbPartHeight(mb_type) is equal to 8, mbPartIdx is equal to 1, and refIdxLXA is equal to refIdxLX, $\text{mvpLX} = \text{mvLXA}$ – MbPartWidth(mb_type) is equal to 8, MbPartHeight(mb_type) is equal to 16, mbPartIdx is equal to 0, and refIdxLXA is equal to refIdxLX, $\text{mvpLX} = \text{mvLXA}$ – MbPartWidth(mb_type) is equal to 8, MbPartHeight(mb_type) is equal to 16, mbPartIdx is equal to 1, and refIdxLXC is equal to refIdxLX, $\text{mvpLX} = \text{mvLXC}$ <p>...</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>8.4.1.3.1 Derivation process for median luma motion vector prediction</p> <p>Inputs to this process are</p> <ul style="list-style-type: none"> – the neighbouring partitions mbAddrN\mbPartIdxN\subMbPartIdxN (with N being replaced by A, B, or C), – the motion vectors mvLXN (with N being replaced by A, B, or C) of the neighbouring partitions, – the reference indices refIdxLXN (with N being replaced by A, B, or C) of the neighbouring partitions, and – the reference index refIdxLX of the current partition. <p>Output of this process is the motion vector prediction mvpLX.</p> <p>The variable mvpLX is derived as follows:</p> <ul style="list-style-type: none"> – When both partitions mbAddrB\mbPartIdxB\subMbPartIdxB and mbAddrC\mbPartIdxC\subMbPartIdxC are not available and mbAddrA\mbPartIdxA\subMbPartIdxA is available, $\text{mvLXB} = \text{mvLXA}$ $\text{mvLXC} = \text{mvLXA}$ $\text{refIdxLXB} = \text{refIdxLXA}$ $\text{refIdxLXC} = \text{refIdxLXA}$ <ul style="list-style-type: none"> – Depending on reference indices refIdxLXA, refIdxLXB, or refIdxLXC, the following applies. <ul style="list-style-type: none"> – If one and only one of the reference indices refIdxLXA, refIdxLXB, or refIdxLXC is equal to the reference index refIdxLX of the current partition, the following applies. Let refIdxLXN be the reference index that is equal to refIdxLX, the motion vector mvLXN is assigned to the motion vector prediction mvpLX: $\text{mvpLX} = \text{mvLXN}$

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<ul style="list-style-type: none"> – Otherwise, each component of the motion vector prediction mvpLX is given by the median of the corresponding vector components of the motion vector mvLXA, mvLXB, and mvLXC: $\text{mvpLX[0]} = \text{Median(mvLXA[0], mvLXB[0], mvLXC[0])}$ $\text{mvpLX[1]} = \text{Median(mvLXA[1], mvLXB[1], mvLXC[1])}$ <p>8.4.1.3.2 Derivation process for motion data of neighbouring partitions</p> <p>Inputs to this process are</p> <ul style="list-style-type: none"> – the macroblock partition index mbPartIdx, – the sub-macroblock partition index subMbPartIdx, – the current sub-macroblock type currSubMbType, – the list suffix flag listSuffixFlag <p>Outputs of this process are (with N being replaced by A, B, or C)</p> <ul style="list-style-type: none"> – mbAddrN\mbPartIdxN\subMbPartIdxN specifying neighbouring partitions, – the motion vectors mvLXN of the neighbouring partitions, and – the reference indices refIdxLXN of the neighbouring partitions. <p>Variable names that include the string "LX" are interpreted with the X being equal to listSuffixFlag.</p> <p>The partitions mbAddrN\mbPartIdxN\subMbPartIdxN with N being either A, B, or C are derived in the following ordered steps.</p> <ol style="list-style-type: none"> 1. Let mbAddrD\mbPartIdxD\subMbPartIdxD be variables specifying an additional neighbouring partition. 2. The process in subclause 6.4.8.5 is invoked with mbPartIdx, currSubMbType, and subMbPartIdx as input and the output is assigned to mbAddrN\mbPartIdxN\subMbPartIdxN with N being replaced by A, B, C, or D. 3. When the partition mbAddrC\mbPartIdxC\subMbPartIdxC is not available, the following applies

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>mbAddrC = mbAddrD</p> <p>mbPartIdxC = mbPartIdxD</p> <p>subMbPartIdxC = subMbPartIdxD</p> <p>The motion vectors mvLXN and reference indices refIdxLXN (with N being A, B, or C) are derived as follows.</p> <ul style="list-style-type: none"> – If the macroblock partition or sub-macroblock partition mbAddrN\mbPartIdxN\subMbPartIdxN is not available or mbAddrN is coded in Intra prediction mode or predFlagLX of mbAddrN\mbPartIdxN\subMbPartIdxN is equal to 0, both components of mvLXN are set equal to 0 and refIdxLXN is set equal to -1. – Otherwise, the following applies. <ul style="list-style-type: none"> – The motion vector mvLXN and reference index refIdxLXN are set equal to MvLX[mbPartIdxN][subMbPartIdxN] and RefIdxLX[mbPartIdxN], respectively, which are the motion vector mvLX and reference index refIdxLX that have been assigned to the (sub-)macroblock partition mbAddrN\mbPartIdxN\subMbPartIdxN. – The variables mvLXN[1] and refIdxLXN are further processed as follows. <ul style="list-style-type: none"> – If the current macroblock is a field macroblock and the macroblock mbAddrN is a frame macroblock $\text{mvLXN}[1] = \text{mvLXN}[1] / 2$ $\text{refIdxLXN} = \text{refIdxLXN} * 2$ – Otherwise, if the current macroblock is a frame macroblock and the macroblock mbAddrN is a field macroblock $\text{mvLXN}[1] = \text{mvLXN}[1] * 2$ $\text{refIdxLXN} = \text{refIdxLXN} / 2$ – Otherwise, the vertical motion vector component mvLXN[1] and the reference index refIdxLXN remain unchanged. <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 148–49).</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
<p>[D] forming a prediction for the first segment with respect to a reference frame based at least in part on the assigned motion vector for the skip coding mode, wherein the assigned motion vector is one of the zero motion vector and the predicted non-zero motion vector.</p>	<p>Each of the Accused Products, such as the ASUS Q543MV, performs a method of decoding an encoded video sequence, the method comprising forming a prediction for the first segment with respect to a reference frame based at least in part on the assigned motion vector for the skip coding mode, wherein the assigned motion vector is one of the zero motion vector and the predicted non-zero motion vector.</p> <p>For example, and without limitation, the H.264/AVC Standard specifies the decoding process for Inter prediction samples in Subclause 8.4.2. The following specifications provide further evidence of how the Accused Products operate:</p> <p>8.4 Inter prediction process</p> <p>This process is invoked when decoding P and B macroblock types.</p> <p>Outputs of this process are Inter prediction samples for the current macroblock that are a 16x16 array predL of luma samples and when chroma_format_idc is not equal to 0 (monochrome) two 8x8 arrays predCr and predCb of chroma samples, one for each of the chroma components Cb and Cr.</p> <p>The partitioning of a macroblock is specified by mb_type. Each macroblock partition is referred to by mbPartIdx. When the macroblock partitioning consists of partitions that are equal to sub-macroblocks, each sub-macroblock can be further partitioned into sub-macroblock partitions as specified by sub_mb_type. Each sub-macroblock partition is referred to by subMbPartIdx. When the macroblock partitioning does not consist of sub-macroblocks, subMbPartIdx is set equal to 0... .</p> <p>The Inter prediction process for a macroblock partition mbPartIdx and a sub-macroblock partition subMbPartIdx consists of the following ordered steps</p> <p>...</p> <ol style="list-style-type: none"> Derivation process for motion vector components and reference indices as specified in subclause 8.4.1.

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>Inputs to this process are</p> <ul style="list-style-type: none"> – a macroblock partition mbPartIdx, – a sub-macroblock partition subMbPartIdx. <p>Outputs of this process are</p> <ul style="list-style-type: none"> – luma motion vectors mvL0 and mvL1 and when chroma_format_idc is not equal to 0 (monochrome) the chroma motion vectors mvCL0 and mvCL1 – reference indices refIdxL0 and refIdxL1 – prediction list utilization flags predFlagL0 and predFlagL1 – the sub-macroblock partition motion vector count subMvCnt. <ol style="list-style-type: none"> 2. The variable MvCnt is incremented by subMvCnt. 3. Decoding process for Inter prediction samples as specified in subclause 8.4.2. <p>Inputs to this process are</p> <ul style="list-style-type: none"> – a macroblock partition mbPartIdx, – a sub-macroblock partition subMbPartIdx. – variables specifying partition width and height for luma and chroma (if available), partWidth, partHeight, partWidthC (if available), and partHeightC (if available) – luma motion vectors mvL0 and mvL1 and when chroma_format_idc is not equal to 0 (monochrome) the chroma motion vectors mvCL0 and mvCL1 – reference indices refIdxL0 and refIdxL1 – prediction list utilization flags predFlagL0 and predFlagL1 <p>Outputs of this process are</p> <ul style="list-style-type: none"> – inter prediction samples (pred); which are a (partWidth)x(partHeight) array predPartL of prediction luma samples and when chroma_format_idc is not equal to 0 (monochrome) two (partWidthC)x(partHeightC) arrays predPartCr, and predPartCb of prediction chroma samples, one for each of the chroma components Cb and Cr. <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 135–36).</p>

EXHIBIT 16**UNITED STATES PATENT No. 7,532,808****CLAIM CHART FOR INFRINGEMENT OF CLAIM 7 BY ASUS ACCUSED PRODUCTS**

U.S. PATENT No. 7,532,808	ASUS ACCUSED PRODUCTS
	<p>8.4.2 Decoding process for Inter prediction samples</p> <p>Inputs to this process are</p> <ul style="list-style-type: none"> – a macroblock partition mbPartIdx, – a sub-macroblock partition subMbPartIdx. – variables specifying partition width and height for luma and chroma (if available), partWidth, partHeight, partWidthC (if available) and partHeightC (if available) – luma motion vectors mvL0 and mvL1 and when chroma_format_idc is not equal to 0 (monochrome) chroma motion vectors mvCL0 and mvCL1 – reference indices refIdxL0 and refIdxL1 <p>Outputs of this process are</p> <ul style="list-style-type: none"> – the Inter prediction samples predPart, which are a (partWidth)x(partHeight) array predPartL of prediction luma samples, and when chroma_format_idc is not equal to 0 (monochrome) two (partWidthC)x(partHeightC) arrays predPartCb, predPartCr of prediction chroma samples, one for each of the chroma components Cb and Cr. <p>...</p> <p>(ITU-T Rec. H.264 (03/2005) Advanced video coding for generic audio visual services at pp. 149–50).</p>